In the Abstract:

~~Integrated circuit arrangement having capacitors and having preferably planar transistors and fabrication method~~

~~An explanation is given, inter alia, of an integrated circuit arrangement (140), which contains a preferably planar transistor (142) and a capacitor (144). The bottom electrode of the capacitor (144) is arranged together with a channel region of the transistor (142) in an SOI substrate. The circuit arrangement (140) is simple to fabricate and has outstanding electronic properties.~~

~~(Figure 13)~~

An integrated circuit arrangement and method of fabricating the integrated circuit arrangement is described. The integrated circuit arrangement contains an insulating region and a sequence of regions which forms a capacitor. The sequence contains a near electrode region near the insulating region, a dielectric region, and a remote electrode region remote from the insulating region. The insulating region is part of an insulating layer arranged in a plane. The capacitor and an active component are arranged on the same side of the insulating layer and form a memory cell. The near electrode region and an active region of the component are arranged in a plane which lies parallel to the plane in which the insulating layer is arranged. A processor is also contained in the integrated circuit arrangement.